REMARKS

Applicants have amended their claims in the above-identified application, in order to further clarify the definition of various aspects of the present invention. Specifically, claim 1 has been amended to recite "at least one" gate electrode, "at least one" source electrode and "at least one" drain electrode. Claim 1 has been further amended to delete the original "wherein" clause, and to recite instead, in a "wherein" clause, that the semiconductor layer is located so as to contact the gate insulating film only at regions which act as channel regions of the IC card apparatus. See, for example, the paragraph bridging pages 7 and 8 of Applicants' specification. In addition, Applicants are adding new claims 2-10 to the application. Claims 2-7 correspond respectively to claims 2-7 of U.S. Patent No. 6,593,977, cited by the Examiner in the Office Action mailed August 30, 2004, in the above-identified application, and which issued from a prior application of the above-identified application being relied upon under 35 USC §120.

New claim 8, dependent on claim 1, recites that the channel regions, in plan view, are between respective source and drain electrodes, that the respective source and drain electrodes contact opposite ends of the semiconductor layer contacting the gate insulating film, and that the at least one gate electrode is above or beneath the semiconductor layer contacting the gate insulating film. Claims 9 and 10 recite subject matter expressly set forth in claims 6 and 2, respectively, but are each dependent on claim 8.

The objection to claim 1 as set forth on page 2 of the Office Action mailed August 30, 2004, is noted. Claim 1 has been amended to recite "at least one ... electrode"; in view of this amendment of claim 1, it is respectfully submitted that the

required correction of claim 1 has been made.

Applicants respectfully traverse the rejection of claim 1 under the second paragraph of 35 USC §112, as being indefinite, as set forth on page 2 of the Office Action mailed August 30, 2004, particularly insofar as this rejection is applicable to the claims as presently amended. Thus claim 1 recites specific functional components; and, moreover, specifies that the semiconductor layer is located so as to contact the gate insulating film only at regions which act as channel regions of the IC card apparatus. Especially in view of the functional recitations, it is respectfully submitted that the claims are complete with respect to the relationships of the elements.

The contention by the Examiner on page 2 of the Office Action mailed August 30, 2004, that the omitted structural cooperative relationships are "gate electrodes, a gate insulating film, source electrodes, drain electrodes, and semiconductor layer", the Examiner contending that there is no structural relationship of these elements, is noted. It is respectfully submitted, however, that by reciting the functionality of the components, any necessary "structural cooperative relationships" are set forth.

In any event, the Examiner's attention is respectfully directed to claim 8 as presently submitted for consideration by the Examiner. Claim 8, dependent on claim 1, defines positioning and structural contact between various of the recited components of the IC card apparatus, including the channel regions, source and drain electrodes, semiconductor layer and the gate electrode. Particularly in view thereof, it is respectfully submitted that claim 8 clearly satisfies the requirements of the second paragraph of 35 USC §112, with respect to structural cooperative relationships of the elements.

The double patenting rejection over claim 1 of prior U.S. Patent No. 6,593,977, set forth on pages 3 and 4 of the Office Action mailed August 30, 2004, is noted. Claim 1 has been amended to delete recitation that the patterned insulating layer is located between the gate insulating film and the semiconductor layer, except for a channel region, and to recite instead that the semiconductor layer is located so as to contact the gate insulating film only at regions which act as channel regions of the IC card apparatus. As present claim 1, the sole independent claim in the above-identified application, is clearly different from claim 1 of U.S. Patent No. 6,593,977, it is respectfully submitted that the double patenting rejection under 35 USC §101 has clearly been overcome.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the reference applied by the Examiner in rejecting claims in the Office Action mailed August 30, 2004, that is, the teachings of U.S. Patent No. 6,025,605 to Lyu, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that this reference as applied by the Examiner would have neither taught nor would have suggested such an IC card apparatus as in the present claims, including, inter alia, the various components set forth in the present claims, and wherein the semiconductor layer is located so as to contact the gate insulating film only at regions which act as channel regions of the IC card apparatus. See claim 1.

In addition, it is respectfully submitted that the applied reference would have neither taught nor would have suggested such an IC card apparatus as in the present

claims, having features as discussed previously in connection with claim 1, and furthermore having additional features as in the remaining claims in the application, including (but not limited to) wherein the semiconductor layer is an organic semiconductor layer (see claims 2 and 10); and/or wherein the channel region has a size which is a same size as a gate electrode, of the at least one gate electrode, of the apparatus (see claims 6 and 9); and/or wherein the patterned insulating layer is a photosensitive insulating film (see claim 3); and/or wherein the substrate is a plastic substrate (see claim 4), particularly one made of polymer material (see clam 5); and/or wherein the patterned insulating layer and gate insulating film are made of different materials (see claim 7).

The present invention is directed to an IC card apparatus, particularly useful with respect to those having organic thin film transistors (organic TFTs).

In forming organic semiconductor films, it has been difficult to form such films with relatively small size (for example, of a size corresponding to a pixel size in a current liquid crystal display apparatus). Thus, as described in the first full paragraph on page 5 of Applicants' specification, since the organic semiconductor film cannot be manufactured finely, an area of the organic semiconductor film is larger than gate electrodes of the TFTs; and an off-current caused by wrap around is increased, the organic semiconductor film cannot be covered by a light shielding layer, and off current with carriers generated by photo-excitation is increased. Moreover, as described in the paragraph bridging pages 4 and 5 of Applicants' specification, where the organic TFT is used for active elements in a liquid crystal display device, writing into a liquid crystal pixel may be produced by an adjacent signal line, and lowering of the contrast results, because a TFT is composed of an organic semiconductor film between the drain

electrode and the adjacent signal line.

Against this background, Applicants provide an apparatus which avoids problems arising in connection with prior TFTs, including organic TFTs. Applicants have found that providing the semiconductor layer so as to contact the gate insulating film only at regions which act as channel regions of the IC card apparatus, the semiconductor layer is provided overlying (or beneath) the gate electrode and having a size, for example, the same as the gate electrode. Thus, the semiconductor film is provided precisely and only in the channel region. Note, for example, the paragraph bridging pages 7 and 8 of Applicants' specification. Note also, for example, the paragraph bridging pages 15 and 16, as well as the remainder of page 16, of Applicants' specification.

Lyu discloses a technique for manufacturing active matrix liquid crystal displays, as well as the displays formed. According thereto, a first metal layer is deposited on a transparent substrate, and gate bus lines and gate electrodes are formed by patterning the first metal layer. A first insulating layer, a semiconductor layer, and a second insulating layer are sequentially deposited on the substrate on which the gate bus line and the gate electrode are formed; and an etch-stopper is formed by patterning the second insulating layer, with an impurity-doped semiconductor layer being deposited on the etch-stopper and the semiconductor layer. A second metal layer is deposited on the impurity-doped semiconductor layer, and the second metal layer, the impurity-doped semiconductor layer and the semiconductor layer are patterned. An insulating passivation layer is deposited on the patterned second metal layer and the first insulating layer. See column 2, lines 24-40 of Lyu; note also Figs. 3A-I and the corresponding description in column 3, line 26 to column 4, line 24, of Lyu.

Noting especially Fig. 3I of Lyu, and in particular the semiconductor layer 137, it can easily be seen that in Lyu the semiconductor layer extends on the gate insulating layer well beyond the channel region. It is respectfully submitted that this reference would have neither disclosed nor would have suggested, and in fact would have taught away from, such an IC card apparatus as in the present claims, including, inter alia, wherein the semiconductor layer is located so as to contact the gate insulating film at regions which act as channel regions of the IC card apparatus, and/or other features of the present invention as discussed previously.

The contention by the Examiner on page 3 of the Office Action mailed August 30, 2004, that Lyu discloses structure wherein a patterned insulating layer 145 is located between the gate insulating film 135 and the semiconductor layer 139, except for a channel region, is noted, but is moot in light of present claim amendments, including the "wherein" clause of claim 1. However, such contention by the Examiner is respectfully traversed. In this regard, note that insulating layer 145 is located above the gate insulating film 135 and the semiconductor layer 137, as well as above the doped semiconductor layer 139. Accordingly, clearly the Examiner errs in stating that in Lyu the patterned insulating layer 145 is between the gate insulating film 135 and the semiconductor layer 139 except for a channel region.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP

Deposit Account No. 01-2135 (Docket No. 503.38289CC2), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
William I. Solomon
Reg. No. 28,565

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666
WIS/sjg